UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/806,871 | 03/22/2004 | Robert Tod Dimpsey | AUS920040064US1 | 2672 |

35525 7590 04/09/2008

IBM CORP (YA)
C/O YEE & ASSOCIATES PC
P.O. BOX 802333
DALLAS, TX 75380

| EXAMINER | |
|---|---|
| SAVLA, ARPAN P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2185 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 04/09/2008 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ptonotifs@yeeiplaw.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/806,871 | DIMPSEY ET AL. | |
| | Examiner | Art Unit | |
| | Arpan P. Savla | 2185 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,4-7,11,12,14-19 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,11,12,14-19 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

This Office action is in response to Applicant's communication filed December 20, 2007 in response to the Office action dated August 24, 2007. Claims 5, 15, and 22 have been amended. Claims 1-2, 4-7, 11-12, 14-19, and 21-25 are pending in this application.

## OBJECTIONS

### *Claims*

1. In view of Applicant's amendment, the objections to **claims 5, 15, and 22** have been withdrawn.

## REJECTIONS BASED ON PRIOR ART

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**3. Claims 1-2, 5-7, 11-12, 15-19, and 22-24 are rejected under 35 U.S.C. 103(a) as being obvious over Matsubara et al. (U.S. Patent 6,381,679) (hereinafter "Matsubara") in view of Anonymously Disclosed, "Method for the dynamic**

**prediction of nonsequential memory accesses" (hereinafter "Anon") and Ishimi (U.S. Patent 5,708,803).**

4. **As per claims 1 and 18**, Matsubara discloses a method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:

responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction (col. 5, lines 1-10; col. 6, lines 35-42 and 53-55; col. 7, lines 10-20; Fig. 1; Fig. 2, elements 21 and 22; Fig. 6B). *It should be noted that computer program product in claims 18-19 and 21-24 executes the exact same functions as the methods in claims 1-2 and 4-7. Therefore, any references that teach claims 1-2 and 4-7 also teach the corresponding claims 18-19 and 21-24. It should also be noted that the "indication bits (i.e. PF bits)" equaling 1 is analogous to the "prefetch indicator being associated with the instruction" and the "CPU 21" is analogous to the "processor unit." Lastly, it should be noted that the "instruction fetch (IF)" stage is when the instruction in the code is loaded into a cache and the "decoding" stage is when the "determination" is made.*

and responsive to the prefetch indicator being associated with the instruction, selectively prefetching data into the cache in the processor (col. 6, lines 53-55; Fig. 2, elements 21 and 22). *It should be noted that when it is determined that the value of the PF bits is 1, all the data of the line is prefetched to the primary cache.*

Matsubara does not expressly disclose a pointer to a data structure identified by the prefetch indicator;

wherein the selectively prefetching step includes:

determining whether outstanding cache misses are present;

and prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold.

Anon discloses a pointer to a data structure identified by the prefetch indicator (General Description, 1st paragraph and 4th paragraph; Detailed Description, 1st paragraph). *It should be noted that the "dynamic prefetch pointer" is analogous to the "pointer to a data structure."*

Matsubara and Anon are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Anon's dynamic prefetch pointer within Matsubara's information processing system.

The motivation for doing so would have been to improve memory access due to improved memory access prediction and also improve performance due to reducing the time spent waiting for memory accesses to complete (Anon, General Description, 5th paragraph).

The combination of Matsubara/Anon does not expressly disclose wherein the selectively prefetching step includes:

determining whether outstanding cache misses are present;

and prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold.

Ishimi discloses wherein the selectively prefetching step includes:

determining whether outstanding cache misses are present (col. 13, line 30; Fig. 13, element S4).

and prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold (col. 13, lines 30-32; Fig. 13, element S10). *It should be noted that the threshold is equal to 1. Thus, when it is determined there is a cache hit, meaning there are zero outstanding cache misses (i.e. the number of outstanding cache misses is than the threshold of 1), data is prefetched.*

The combination of Matsubara/Anon and Ishimi are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Ishimi's fetch mechanism within Matsubara/Anon's information processing system.

The motivation for doing so would have been to provide a data processor capable of processing quickly by lessening the number of abortions even when a branch prediction is preformed (Ishimi, col. 3, lines 3-6).

Therefore, it would have been obvious to combine Matsubara, Anon, and Ishimi for the benefit of obtaining the invention as specified in claims 1 and 18.

5. **As per claims 2 and 19**, the combination of Matsubara/Anon/Ishimi discloses the prefetch indicator contains the pointer to the data structure (Anon, General Description, 4th paragraph).

6. **As per claims 5 and 22**, the combination of Matsubara/Anon/Ishimi discloses

the processor unit is selected from one of an instruction cache, data cache, and a load/store unit (Matsubara, col. 6, lines 35-42; col. 7, lines 10-20; Fig. 2, element 21). *It should be noted that the "CPU 21" is analogous to a "load/store unit."*

7. **As per claims 6 and 23**, the combination of Matsubara/Anon/Ishimi discloses the cache is an instruction cache (Ishimi, col. 1, lines 25-28).

8. **As per claims 7 and 24**, the combination of Matsubara/Anon/Ishimi discloses the cache is a data cache (Matsubara, col. 8, lines 56-63).

9. **As per claim 11**, Matsubara discloses a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the data processing system comprising:

determining means, responsive to loading an instruction in the code into a cache, for determining, by the a processor unit, whether a prefetch indicator is associated with the instruction (col. 5, lines 1-10; col. 6, lines 35-42 and 53-55; col. 7, lines 10-20; Fig. 1; Fig. 2, elements 21 and 22; Fig. 6B); *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 1 and 18 above.*

and selectively prefetching means, responsive to the prefetch indicator being associated with the instruction, for selectively prefetching data into the cache in the processor (col. 6, lines 53-55; Fig. 2, elements 21 and 22). *It should be noted that pg. 13, lines 3-5 of Applicant's specification appear to define this means as a computer. Also, see the citation note for the similar limitation in claims 1 and 18 above.*

Matsubara does not expressly disclose a pointer to a data structure identified by

the prefetch indicator;

wherein the selectively prefetching means includes:

means for determining whether outstanding cache misses are present;

and means for prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold.

Anon discloses a pointer to a data structure identified by the prefetch indicator (General Description, 1st paragraph and 4th paragraph; Detailed Description, 1st paragraph). *See the citation note for the similar limitation in claims 1 and 18 above.*

Matsubara and Anon are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Anon's dynamic prefetch pointer within Matsubara's information processing system.

The motivation for doing so would have been to improve memory access due to improved memory access prediction and also improve performance due to reducing the time spent waiting for memory accesses to complete (Anon, General Description, 5th paragraph).

The combination of Matsubara/Anon does not expressly disclose wherein the selectively prefetching means includes:

means for determining whether outstanding cache misses are present;

and means for prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold.

Ishimi discloses wherein the selectively prefetching means includes:

means for determining whether outstanding cache misses are present (col. 13, line 30; Fig. 13, element S4).

and means for prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold (col. 13, lines 30-32; Fig. 13, element S10). *See the citation note for the similar limitation in claims 1 and 18 above.*

The combination of Matsubara/Anon and Ishimi are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Ishimi's fetch mechanism within Matsubara/Anon's information processing system.

The motivation for doing so would have been to provide a data processor capable of processing quickly by lessening the number of abortions even when a branch prediction is preformed (Ishimi, col. 3, lines 3-6).

Therefore, it would have been obvious to combine Matsubara, Anon, and Ishimi for the benefit of obtaining the invention as specified in claim 11.

10. **As per claim 12**, the combination of Matsubara/Anon/Ishimi discloses the prefetch indicator contains the pointer to the data structure (Anon, General Description, 4th paragraph).

11. **As per claim 15**, the combination of Matsubara/Anon/Ishimi discloses the processor unit is selected from one of an instruction cache, data cache, and a load/store unit (Matsubara, col. 6, lines 35-42; col. 7, lines 10-20; Fig. 2, element 21). *See the*

*citation note for claims 5 and 22 above.*

12. **As per claim 16**, the combination of Matsubara/Anon/Ishimi discloses the cache is an instruction cache (Ishimi, col. 1, lines 25-28).

13. **As per claim 17**, the combination of Matsubara/Anon/Ishimi discloses the cache is a data cache (Matsubara, col. 8, lines 56-63).

**14. Claims 4, 14, and 21 are rejected under 35 U.S.C. 103(a) as being obvious over Matsubara in view of Anon and Ishimi as applied to claims 1, 11, and 18 above, and further in view of Hooker (U.S. Patent Application Publication 2003/0191900).**

15. **As per claims 4 and 21**, the combination of Matsubara/Anon/Ishimi discloses all the limitations of claims 4 and 21 except wherein the selectively prefetching step further includes:

determining whether to replace cache lines;

and prefetching the in response to a determination that a number of cache lines chosen to replaced is greater than a threshold.

Hooker discloses wherein the selectively prefetching step further includes:

determining whether to replace cache lines (paragraph 0069; Fig. 5, element 536); *It should be noted that the "response buffers" are analogous to the "cache lines."*

and prefetching the in response to a determination that a number of cache lines chosen to replaced is greater than a threshold (paragraph 0070; Fig. 5, element 538).

The combination of Matsubara/Anon/Ishimi and Hooker are analogous art because they are from the same field of endeavor, that being prefetching memory

systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Hooker's threshold based prefetch method into Matsubara/Anon/Ishimi's information processing system.

The motivation for doing so would have been to reduce software code size over conventional single-cache line prefetch instructions because fewer prefetch instructions need to be included in the program (Hooker, paragraph 0018). Another motivation for doing so would have been to potentially improve system performance by making more efficient use of the processor bus than the conventional method (Hooker, paragraph 0018). Lastly, another motivation for doing so would have been to potentially improve processing performance by moving data into the microprocessor cache more efficiently than the conventional method by alleviating the problems caused by the fact that a range of core clock to processor bus clock ratios may exist (Hooker, paragraph 0018).

Therefore, it would have been obvious to combine Matsubara, Anon, Ishimi, and Hooker for the benefit of obtaining the invention as specified in claims 4 and 21.

16. **As per claim 14**, the combination of Matsubara/Anon/Ishimi/Hooker discloses wherein the selectively prefetching means further includes:

means for determining whether to replace cache lines (paragraph 0069; Fig. 5, element 536); *See the citation note for claims 4 and 21 above.*

and means for prefetching the in response to a determination that a number of cache lines chosen to replaced is greater than a threshold (paragraph 0070; Fig. 5, element 538).

**17. Claim 25 is rejected under 35 U.S.C. 103(a) as being obvious over Matsubara in view of Anon, Ishimi, and Hooker.**

18. **As per claim 25**, Matsubara discloses a method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:

responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction (col. 5, lines 1-10; col. 6, lines 35-42 and 53-55; col. 7, lines 10-20; Fig. 1; Fig. 2, elements 21 and 22; Fig. 6B), wherein the processor unit is selected from one of an instruction cache, data cache, or a load/store unit (Matsubara, col. 6, lines 35-42; col. 7, lines 10-20; Fig. 2, element 21).

and responsive to the prefetch indicator being associated with the instruction, selectively prefetching data into the cache in the processor (col. 6, lines 53-55; Fig. 2, elements 21 and 22).

Matsubara does not expressly disclose a pointer to a data structure identified by the prefetch indicator;

wherein the selectively prefetching step includes:

determining whether outstanding cache misses are present;

and prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold, and wherein the selectively prefetching step further includes:

determining whether to replace cache lines;

and prefetching the in response to a determination that a number of cache lines chosen to replaced is greater than a threshold.

Anon discloses a pointer to a data structure identified by the prefetch indicator (General Description, 1st paragraph and 4th paragraph; Detailed Description, 1st paragraph). *See the citation notes from the similar limitations in claims 1 and 18 above.*

Matsubara and Anon are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Anon's dynamic prefetch pointer within Matsubara's information processing system.

The motivation for doing so would have been to improve memory access due to improved memory access prediction and also improve performance due to reducing the time spent waiting for memory accesses to complete (Anon, General Description, 5th paragraph).

The combination of Matsubara/Anon does not expressly disclose wherein the selectively prefetching step includes:

determining whether outstanding cache misses are present;

and prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold, and wherein the selectively prefetching step further includes:

determining whether to replace cache lines;

and prefetching the in response to a determination that a number of cache lines chosen to replaced is greater than a threshold.

Ishimi discloses wherein the selectively prefetching step includes:

determining whether outstanding cache misses are present (col. 13, line 30; Fig. 13, element S4).

and prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold (col. 13, lines 30-32; Fig. 13, element S10).

The combination of Matsubara/Anon and Ishimi are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Ishimi's fetch mechanism within Matsubara/Anon's information processing system.

The motivation for doing so would have been to provide a data processor capable of processing quickly by lessening the number of abortions even when a branch prediction is preformed (Ishimi, col. 3, lines 3-6).

The combination of Matsubara/Anon/Ishimi does not expressly disclose wherein the selectively prefetching step further includes:

determining whether to replace cache lines;

and prefetching the in response to a determination that a number of cache lines chosen to replaced is greater than a threshold.

Hooker discloses wherein the selectively prefetching step further includes:

determining whether to replace cache lines (paragraph 0069; Fig. 5, element 536);

and prefetching the in response to a determination that a number of cache lines chosen to replaced is greater than a threshold (paragraph 0070; Fig. 5, element 538).

The combination of Matsubara/Anon/Ishimi and Hooker are analogous art because they are from the same field of endeavor, that being prefetching memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Hooker's threshold based prefetch method into Matsubara/Anon/Ishimi's information processing system.

The motivation for doing so would have been to reduce software code size over conventional single-cache line prefetch instructions because fewer prefetch instructions need to be included in the program (Hooker, paragraph 0018). Another motivation for doing so would have been to potentially improve system performance by making more efficient use of the processor bus than the conventional method (Hooker, paragraph 0018). Lastly, another motivation for doing so would have been to potentially improve processing performance by moving data into the microprocessor cache more efficiently than the conventional method by alleviating the problems caused by the fact that a range of core clock to processor bus clock ratios may exist (Hooker, paragraph 0018).

Therefore, it would have been obvious to combine Matsubara, Anon, Ishimi, and Hooker for the benefit of obtaining the invention as specified in claim 25.

## ***Response to Arguments***

19. Applicant's arguments filed December 20, 2007 with respect to **claims 1-2, 4-7, 11-12, 14-19, and 21-24** have been fully considered but they are not persuasive.

20. With respect to Applicant's argument in the first full paragraph on page 8 and the first, second, and third full paragraphs on page 9 of the communication filed December 20, 2007, the Examiner respectfully disagrees. Ishimi, Fig. 13, element S4 shows a determination is made as to whether there is a cache hit or a cache miss. In the case of a cache hit, data is fetched from cache. It is important to realize that when it is determined there is a cache hit, it is also implicitly determined there are zero outstanding cache misses. Thus, it follows that fetching data from cache in response to a cache hit equates to fetching data from cache in response to a determination that the number of outstanding cache misses is zero. It also follows that fetching data from cache in response to a determination that the number of outstanding cache misses is zero implicitly discloses the use of a threshold value because the fetching of data from cache only occurs when the number of outstanding cache misses is less than this implicit threshold, that threshold value being 1.

When taking the broadest reasonable interpretation of Applicant's claim language, there is clearly a situation when Applicant's "threshold" is equal to 1. Since data is prefetched in response to a determination that a number of outstanding cache misses is less than a threshold, in this situation when the threshold is equal to 1, it follows that data is prefetched in response to a determination that a number of outstanding cache misses is zero. As described in the paragraph directly above, Ishimi

discloses such a situation. Accordingly, when taking the broadest reasonable interpretation of the claim language, in the situation when Applicant's threshold is equal to 1, Ishimi sufficiently discloses prefetching data in response to a determination that a number of outstanding cache misses is less than a threshold.

21. With respect to Applicant's argument in the fourth full paragraph on page 9 of the communication filed December 20, 2007, the Examiner respectfully disagrees. As detailed directly above in section 20 of the current Office action, Ishimi sufficiently discloses prefetching data in response to a determination that a number of outstanding cache misses is less than a threshold, thus, the combination of Matusbara/Anon/Ishimi sufficiently discloses all the features of claim 1.

22. With respect to Applicant's argument beginning in the last full paragraph on page 9 through the first paragraph on page 10 of the communication filed December 20, 2007, the Examiner respectfully disagrees. The need, reason, and/or motivation to combine Matsubara with Anon is because Anon provides the advantage of improving memory access due to improved memory access prediction and also improving performance due to reducing the time spent waiting for memory accesses to complete. Therefore, the Examiner has provided proper motivation to combine the teachings of Matsubara and Anon. The need, reason, and/or motivation for combining Ishimi with the combination of Matsubara/Anon is because Ishimi provides the advantage of a data processor capable of processing quickly by lessening the number of abortions even when a branch prediction is preformed. Therefore, the Examiner has provided proper motivation to combine the teachings of Matsubara/Anon and Ishimi. Accordingly, the

Examiner has satisfied the requirement of articulating a reason with some rational underpinning to support the legal conclusion of obviousness as required under *KSR* as to why one of ordinary skill in the art would look to combine the teachings of Matsubara and Anon as well as the teachings of Matsuabara/Anon and Ishimi. Consequently, the Examiner's obviousness rejections are sustained.

23. As for Applicant's arguments with respect to independent claims 11, 18, and 25, the arguments rely on the allegation that independent claims 1 allowable and therefore for the same reasons independent claims 11, 18, and 25 are allowable. However, as addressed above, independent claim 1 is not allowable, thus, Applicant's arguments with respect to independent claims 11, 18, and 25 are not persuasive.

24. As for Applicant's arguments with respect to the dependent claims, the arguments rely on the allegation that the independent claims are allowable and therefore, by virtue of their dependency, the dependent claims are allowable. However, as addressed above, the independent claims are not allowable, thus, Applicant's arguments with respect to the dependent claims are not persuasive.

## ***Conclusion***

**STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

**CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, **claims 1-2, 4-7, 11-12, 14-19, and 21-25** have received a second action on the merits and are subject of a second action final.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571)272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
March 23, 2008

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185